## ABSTRACT OF THE DISCLOSURE

A processor (e.g., a co-processor) comprising a decoder adapted to decode instructions from a first instruction set in a first mode and a second instruction set in a second mode. A pre-decoder coupled to the decoder, and operates in parallel with the decoder, determines if subsequent instructions switches the decoder from one mode to the other temporarily or permanently. In particular, the pre-decoder examines at least five Bytecodes concurrently with the decoder decoding a current instruction from a particular instruction set. If the pre-decoder determines that at least one of the five Bytecodes includes a predetermined instruction, the predetermined instruction is skipped and a following instruction is loaded into the decode logic and the decode logic switches from one mode to the other for the decoding of at least the following instruction.